REMARKS

Claims 1-12 are pending in the present application. Claims 1, 4, 5, 8, 9, 11 and 12 have been amended.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

Enclosed is one (1) red-inked Drawing Annotated Sheet, wherein the dicing tape has been denoted as "66", to improve consistency. Also enclosed is one (1) Drawing Replacement Sheet, incorporating the above noted drawing correction. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the Drawing Replacement Sheet.**

Specification

A new title has been required which is more clearly indicative of the invention to which the claims are directed. Accordingly, the title of the application has been amended as "A DICED SEMICONDUCTOR DEVICE HAVING NARROW KERF AREA". The Examiner is respectfully requested to approve the amended title, or to suggest a more appropriate title.

Claim Rejections-35 U.S.C. 102

Claims 1, 5 and 9 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Ohsumi et al. reference (U.S. Patent No. 6,303,470). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 1 includes in combination an electrode pad formed over the substrate; and a seal layer which seals a semiconductor element formed on the substrate, "wherein a side surface of the seal layer is positioned inside a side surface of the substrate, the electrode pad is formed next to the side surface of the seal layer, and the side surface of the substrate and the side surface of the seal layer are located along a substrate grid line". The semiconductor device in accordance with claim 1 has the advantage of high reliability, because peeling of electrodes during dicing is prevented.

The Examiner has relied upon Figs. 2(E) and 13(F) of the Ohsumi et al. reference as disclosing the features of claim 1. However, Fig. 2(E) of the Ohsumi et al. reference does not disclose a side surface of a seal layer positioned inside of a side surface of a substrate, wherein the side surface of the substrate and the side surface of the seal layer are both located along a substrate grid line, as would be necessary to meet the features of claim 1. A substrate grid line is not specifically described with respect to Figs. 2(A) – 2(E) of the Ohsumi et al. reference.

Also, as described beginning in column 5, line 48 of the Ohsumi et al. reference

with respect to Figs. 13(A) – 13(F), circuit elements 201 are formed on semiconductor wafer 202, which includes grid lines 203 arranged between circuit elements 201. Since the semiconductor wafer in Figs. 13(A) – 13(F) of the Ohsumi et al. reference is depicted prior to dicing, only an outermost peripheral side edge of semiconductor wafer 202 is shown. The structures in Figs. 13(A) – 13(F) of the Ohsumi et al. reference do not include a side surface of a substrate located along a substrate grid line. Accordingly, Applicant respectfully submits that the semiconductor device of claim 1 distinguishes over the Ohsumi et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 1, is improper for at least these reasons.

The semiconductor device of claim 5 includes in combination an electrode pad formed over the substrate; and a sealing resin sealing a semiconductor element formed on the substrate, "wherein a side surface of the sealing resin is positioned inside of a side surface of the substrate, the electrode pad is formed next to the side surface of the sealing resin, and the side surface of the substrate and the side surface of the sealing resin are located along a substrate grid line".

Applicant respectfully submits that the semiconductor device of claim 5 distinguishes over the Ohsumi et al. reference as relied upon by the Examiner for at least somewhat similar reasons as set forth above. Particularly, a grid line is not specifically described with respect to Fig. 2(E) of the Ohsumi et al. reference. Moreover, since semiconductor wafer 202 in Fig. 13(F) of the Ohsumi et al. reference is depicted prior to dicing, a side surface of a substrate is not shown as located along a

substrate grid line. Applicant therefore respectfully submits that claim 5 distinguishes over the Ohsumi et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 5, is improper for at least these reasons.

The semiconductor device of claim 9 includes in combination an electrode pad; a wiring; a sealing resin; and an external terminal, "wherein an edge of the sealing resin is formed inside an edge of the substrate, the electrode pad is formed next to the edge of the sealing resin, and the edge of the substrate and the edge of the sealing resin are located along a substrate grid line".

Applicant respectfully submits that the semiconductor device of claim 9 distinguishes over the Ohsumi et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 9, is improper for at least somewhat similar reasons as set forth above.

Claims 1, 4, 5, 8, 9 and 12 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Satoh et al. reference (U.S. Patent Application Publication No. 2002/0025655). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The Examiner has relied on Fig. 1 of the Satoh et al. reference as disclosing the features of the claims. However, electrode pad 2 in Fig. 1 of the Satoh et al. reference is formed in a central portion of the semiconductor device. Electrode pad 2 in Fig. 1 of the Satoh et al. reference is not formed next to a side surface of a seal layer, wherein a side surface of the substrate and the side surface of the seal layer are located along a

substrate grid line. Applicant therefore respectfully submits that the semiconductor device of claim 1 distinguishes over the Satoh et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1 and 4, is improper for at least these reasons.

Applicant also respectfully submits that claims 5 and 9 each respectively distinguish over the Satoh et al. reference for at least somewhat similar reasons as set forth above. Applicant therefore respectfully submits that this rejection, insofar as it may pertain to claims 5, 8, 9 and 12, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 2, 3, 6, 7, 10 and 11 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Satoh et al. reference, in further view of cited case law. Applicant respectfully submits that these claims distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, at least by virtue of respective dependency upon claims 1, 5 and 9.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: One (1) Drawing Annotated Sheet
One (1) Drawing Replacement Sheet

OIPE JC151
DEC 29 2004
PATENT & TRADEMARK OFFICE

ANNOTATED SHEET

Fig. 8A

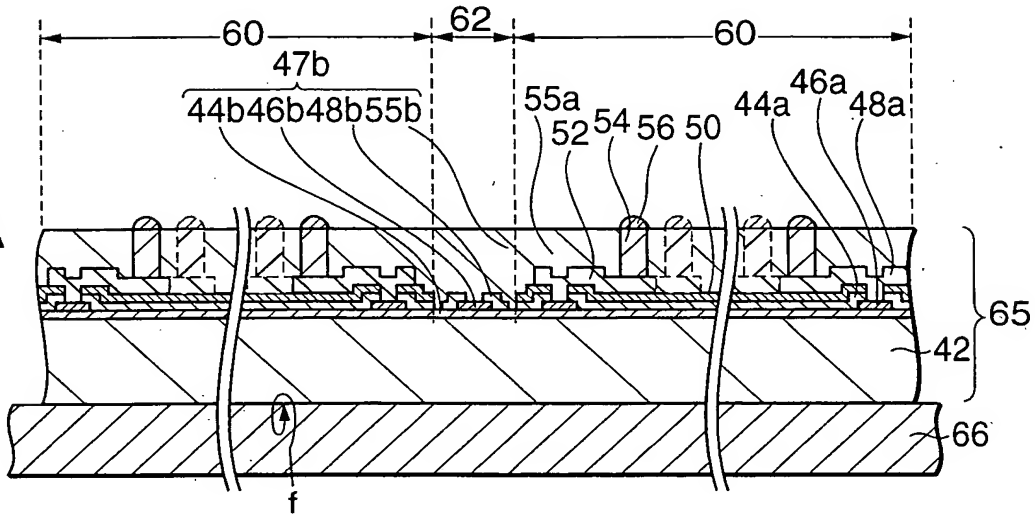

Fig. 8B

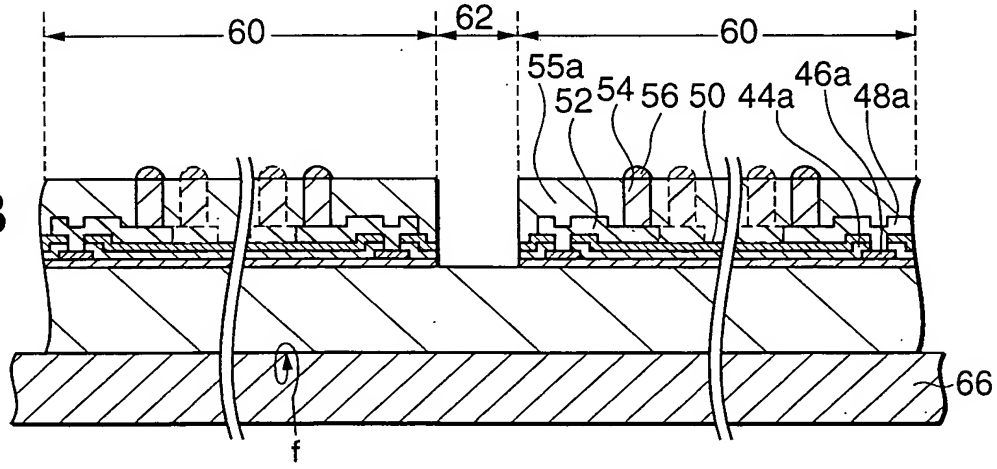

Fig. 8C